Detector Support Group

We choose to do these things "not because they are easy, but because they are hard".

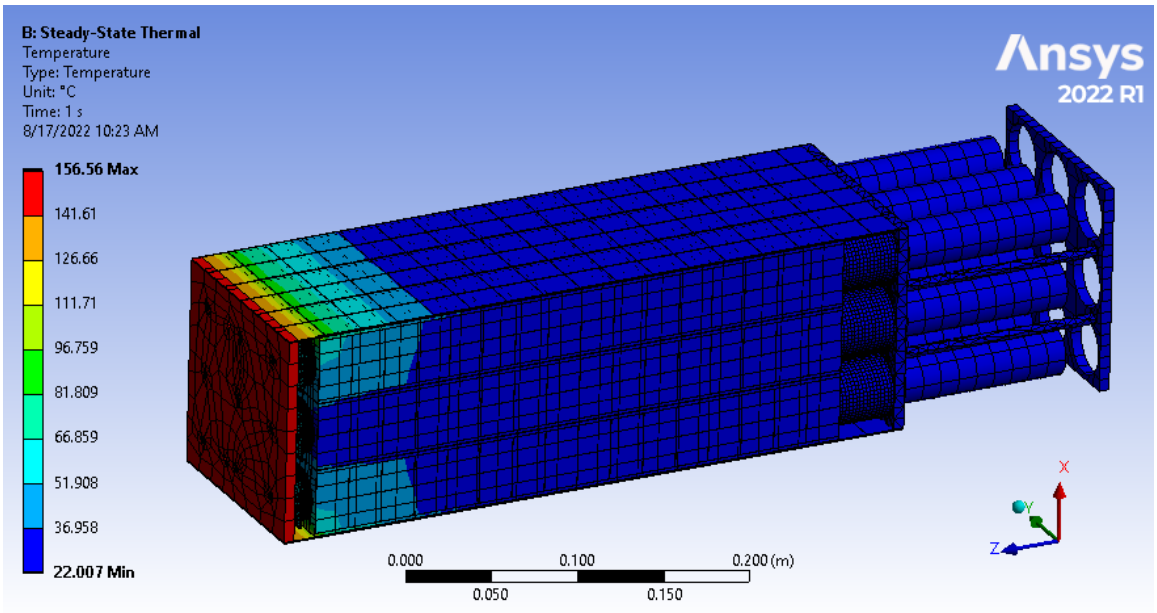
Weekly Report, 2022-08-17

Summary

Hall A – ECal

George Jacobs, Mindy Leffel, Tyler Lemon, and Marc McMullen

- Developing Ansys steady-state thermal model for heating a supermodule using thermal tape on its end plate
  - ✶ Applied 100 W of heat to end plate of module
  - ✶ Temperature at end plate rises to ~156°C, but the very small contact area between end plate and other parts results in heat quickly dissipating so most of supermodule remains close to ambient temperature
  - ✶ Suspect that model will have to use Ansys Fluent to consider heating of air in gaps around supermodule



Steady-state thermal analysis results with 100 W of heat applied to end plate of supermodule

Hall A – GEn-II

Mindy Leffel

- Fabricated and tested five twisted pair cables; 26 of 42 complete

Hall A – SoLID

Pablo Campero, Brian Eng, Mindy Leffel, and Marc McMullen

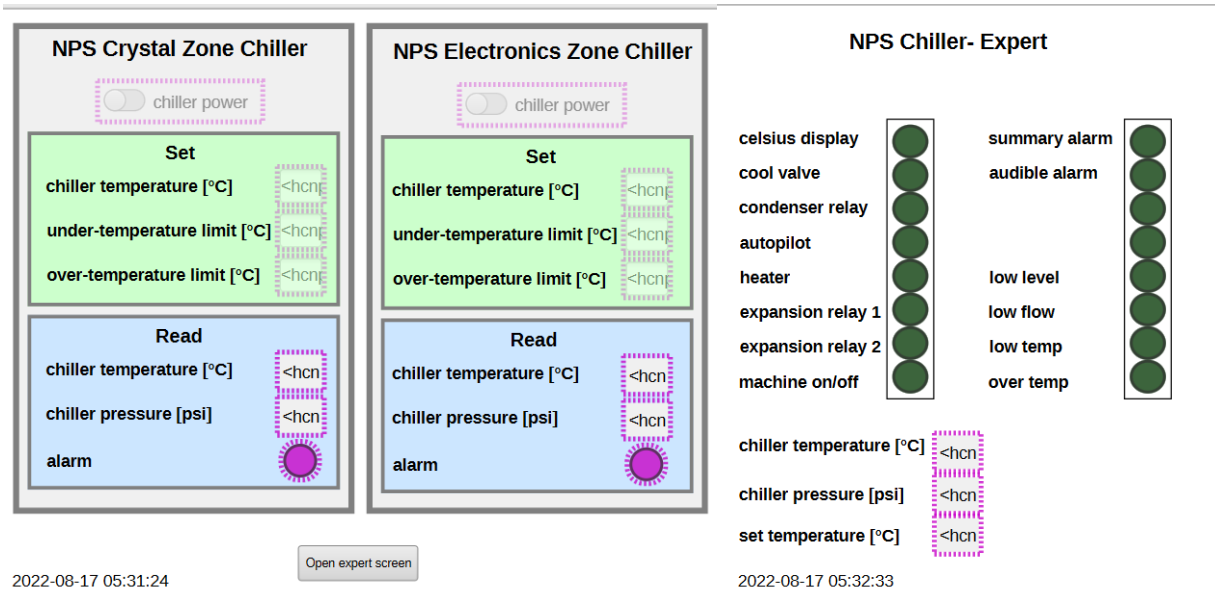
- Repaired transposed wires on JT valve connector

Hall C – NPS

Mary Ann Antonioli, Peter Bonneau, Aaron Brown, Pablo Campero, Brian Eng, George Jacobs, Mindy Leffel, Tyler Lemon, and Marc McMullen

- Created LabVIEW network variables and EPICS process variables for the chillers

- Generated two chiller Phoebus screens, Main and Expert, for one chiller – tested and debugged; works as expected
- Adding second chiller inputs and readback to each screen



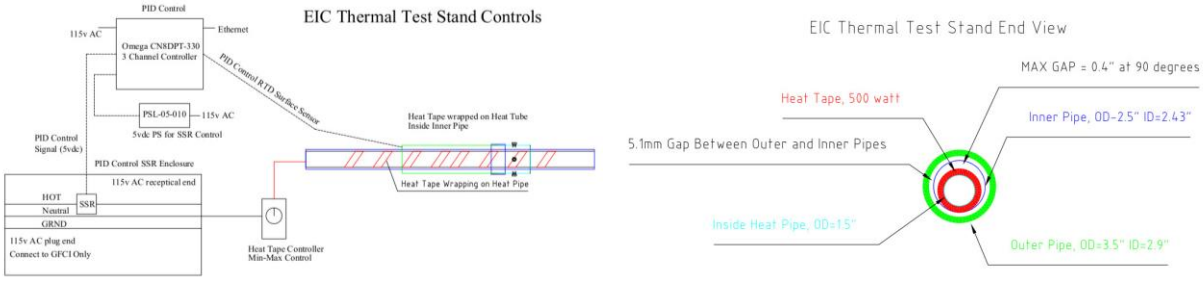
Main screen with both chillers (left); Expert screen for one chiller (right), to be updated with second chiller

- Updating process variable spreadsheet with LabVIEW variable name, data type, number of elements in arrays, and Phoebus screen name
- Adding HV controls and monitoring Phoebus screens to the Hall C NPS computer (*cdaql3*)
  - ✶ Debugging and revising screens as needed to ensure they work as expected in the Hall C computing environment
- Investigating VME LED Driver (VLD) test stand
  - ✶ Received VME controller from DAQ group
  - ✶ Was able to read VLD registers, but first one didn't match the manual due to old firmware
- Debugged cRIO's serial communication using NI-9870 serial modules
- Tested and debugged cRIO communication to Keysight mainframe
  - ✶ cRIO can communicate to mainframe through a USB connection
  - ✶ Depending on final location of Keysight mainframe and cRIO in Hall C, a USB repeater cable may be needed for connection
    - ▪ If Keysight mainframe and cRIO are extremely far apart (> 50 ft.), will have to revert back to using serial-to-GPIB converter
- Continued working on 52-pin Radiall connector to SHV adapter
  - ✶ Wired 12 cables; 36 of 48 complete

EIC

Pablo Campero, Brian Eng, and George Jacobs

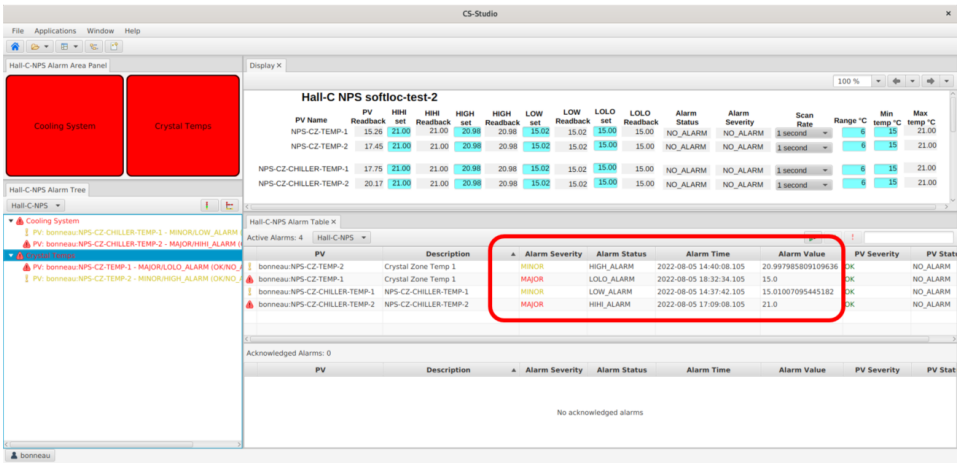
- Developing beam pipe test setup – thermal test heater controls



DSG R&D – EPICS Alarm System

Peter Bonneau

- Conducting PV alarm latch testing using the Phoebus alarm test system
  - ✶ An EPICS softIOC simulates four temperatures from the crystal zone chiller, electronics zone chiller, and crystal thermocouples
  - ✶ Using the test system user interface, the PV alarm configurations were set to enable alarm latching and PV value thresholds were set allowing all levels and severities of alarms
  - ✶ The alarm system correctly latched HIHI, HIGH, LOW, and LOLO levels of alarms
    - The PV value and the time of the alarm was latched correctly
    - The latched alarms were held continuously until acknowledged by the user



Phoebus Alarm Test System User Interface with latched HIHI, HIGH, LOW, and LOLO